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10/645,024

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James Allan Kahle

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7352

7590

10/04/2006

Gregory W. Carr
670 Founders Square
900 Jackson Street
Dallas, TX 75202

EXAMINER

BUTLER, DENNIS

ART UNIT

PAPER NUMBER

2115

DATE MAILED: 10/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/645,024

Applicant(s)

KAHLE ET AL.

Examiner

Dennis M. Butler

Art Unit

2115

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 July 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 16-36 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 16-36 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date. _____ | 6) <input type="checkbox"/> Other: _____ |

Art Unit: 2115

1. This action is in response to the amendment received on July 14, 2006. Claims 16-36 are pending. Claims 1-15 have been canceled. Claims 16-36 have been added based on applicant's election of Group IV in response to the restriction requirement.

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 25-32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 25, the phrase "the subunit" lacks proper antecedent basis because the preceding phrase describes that the processor has a plurality of subunits and it is unclear which subunit the phrase refers to. In addition, the phrase "the predetermined bit position" lacks proper antecedent basis because the preceding phrase describes that the control register has a plurality of predetermined bit positions and it is unclear which predetermined bit position the phrase refers to.

Claims 26-32 are rejected because they incorporate the deficiencies of claim 25.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Art Unit: 2115

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 16-23, 25-31 and 33-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Takashima et al., U. S. Patent Application Publication 2003/0135779.

Per claims 16 and 33:

A) Takashima et al teach the following claimed items:

1. a control register with the register comprising the bus width mode area 148 and the operation mode area 149 of figure 1 and/or the specific register and at paragraphs 65 and 167;

2. determining an idle (unused) status of a subunit (partial calculation units 132 a-c) of the processor based on the control register with bus width mode area 148 and bus width controlling unit 170 of figure 1, with partial calculation units 132 a-c of figure 2 and at paragraphs 13, 65-69 and 76-78;
3. providing a clock signal to the subunit based on the determined idle (unused) status with figures 2 and 3 and at paragraph 69;
4. providing a voltage to the subunit based on the determined idle (unused) status with figure 1 and at paragraph 68.

Per claims 17-23 and 34-36:

Takashima describes including a bus width mode area 148 and an operation mode area 149 in the control register and also describes including a specific register with the same areas at paragraphs 65 and 167. These areas comprise architected bits that indicate the bus width mode in the bus width mode area and architected bits that indicate the operation mode in the operation mode area.

Therefore, the register corresponds to the claimed machine state register.

Takashima describes that the bus width mode area/bits indicate whether the calculation unit operates in an 8-bit, 12-bit or 16-bit mode in paragraph 66.

Takashima describes that the 8-bit, 12-bit or 16-bit bus width modes determine which of the subunits 132 a-c of the calculation unit are active or powered at paragraphs 71 and 76-78. Therefore, at least one bit in the bus width mode area is associated with at least one subunit (partial calculation unit). Takashima describes reading at least one bit associated with at least one subunit with figure

1 and at paragraph 71. Takashima describes setting one or more bits based on an idle (unused) status of a subunit with figure 1 and at paragraphs 60-61 and 66-67. Takashima describes data flow circuitry comprising a plurality of sections with at least one section configured as a subunit with partial calculation units 132 a-c of figure 2 and at paragraphs 76-78. Takashima describes partitioned upper (15:12) and lower (7:0) bit data register circuitry portions configured as a subunit with the registers storing the scrA and scrB data bits (15:0) of figure 2, with figure 8 and at paragraphs 76-78 and 146-148. Takashima describes a partitioned ALU comprising an upper ALU (partial calculation unit 132c) and a lower ALU (partial calculation unit 132a) configured as subunits with instruction execution unit 130 of figure 1 and at paragraphs 63 and 64.

Per claim 25:

A) Takashima et al teach the following claimed items:

1. a software accessible control register having predetermined bit positions indicating subunits (partial calculation units 132 a-c) of the processor with the register comprising the bus width mode area 148 and the operation mode area 149 of figure 1 and/or the specific register, with figure 2 and at paragraphs 65-67, 76-78 and 167;
2. a local clock buffer coupled to the control register to provide a clock to the subunit based on the predetermined bit position associated with the subunit with frequency control unit 160 of figure 1 and clock gating unit 136 of figure 2 and at paragraphs 69 and 82;

3. a voltage signal coupled to the control register to provide a voltage to the subunit based on the predetermined bit position associated with the subunit at paragraph 68.

Regarding the predetermined bit positions indicating subunits, Takashima describes including a bus width mode area 148 and an operation mode area 149 in the control register and also describes including a specific register with the same areas at paragraphs 65 and 167. These areas comprise predetermined bit positions that indicate the bus width mode in the bus width mode area and predetermined bit positions that indicate the operation mode in the operation mode area. Takashima describes that the bus width mode area/bit positions indicate whether the calculation unit operates in an 8-bit, 12-bit or 16-bit mode in paragraph 66. Takashima describes that the 8-bit, 12-bit or 16-bit bus width mode bit positions determine which of the subunits 132 a-c of the calculation unit are active or powered at paragraphs 71 and 76-78. Therefore, the predetermined bit positions in the bus width mode area indicate subunits (partial calculation units).

Per claims 26-31:

Takashima describes including a bus width mode area 148 and an operation mode area 149 in the control register and also describes including a specific register with the same areas at paragraphs 65 and 167. These areas comprise architected bits that indicate the bus width mode in the bus width mode area and architected bits that indicate the operation mode in the operation mode area.

Therefore, the register corresponds to the claimed machine state register.

Takashima describes that the bus width mode area/bits indicate whether the calculation unit operates in an 8-bit, 12-bit or 16-bit mode in paragraph 66.

Takashima describes that the 8-bit, 12-bit or 16-bit bus width modes determine which of the subunits 132 a-c of the calculation unit are active or powered at paragraphs 71 and 76-78. Therefore, at least one bit in the bus width mode area is associated with at least one subunit (partial calculation unit). Takashima describes reading at least one bit associated with at least one subunit with figure 1 and at paragraph 71. Takashima describes setting one or more bits based on an idle (unused) status of a subunit with figure 1 and at paragraphs 60-61 and 66-67. Takashima describes data flow circuitry comprising a plurality of sections with at least one section configured as a subunit with partial calculation units 132 a-c of figure 2 and at paragraphs 76-78. Takashima describes partitioned upper (15:12) and lower (7:0) bit data register circuitry portions configured as a subunit with the registers storing the scrA and scrB data bits (15:0) of figure 2, with figure 8 and at paragraphs 76-78 and 146-148. Takashima describes a partitioned ALU comprising an upper ALU (partial calculation unit 132c) and a lower ALU (partial calculation unit 132a) configured as subunits with instruction execution unit 130 of figure 1 and at paragraphs 63 and 64.

8. Claims 24 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takashima et al., U. S. Patent Application Publication 2003/0135779.

Per claims 24 and 32:

Takashima teaches the elements of claims 16 and 25 as described in the above rejection. The claims differ from Takashima in that Takashima fails to explicitly teach the processor comprising a floating point unit (FPU) configured as a subunit as claimed. However, Takashima describes that the processor comprises calculation circuits such as arithmetic circuits including adding and multiplying circuits and logic circuits with instruction execution unit 130 of figure 1 and at paragraphs 63 and 64. FPUs are a well known component of processor and it would have been obvious to one having ordinary skill in the art at the time the invention was made to include a FPU as a subunit of the processor, in view of Takashima's teaching of including a multiplying circuit, in order to perform floating point operations.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis M. Butler whose telephone number is 571-272-3663. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Application/Control Number: 10/645,024

Page 9

Art Unit: 2115

Dennis M. Butler

Dennis M. Butler
Primary Examiner
Art Unit 2115